# 2N7002E

## List

# 2N7002E

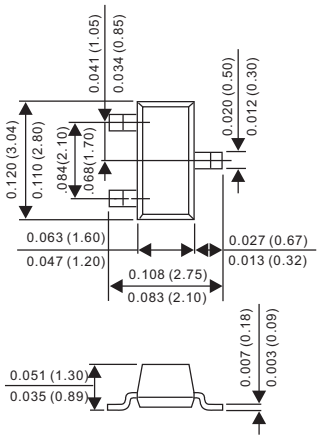
## 60V N-Channel Enhancement Mode MOSFET

## Features

- 60V / 0.50A , $R_{DS(ON)}$= 5.0Ω@$V_{GS}$=10V
- 60V / 0.30A , $R_{DS(ON)}$= 5.5Ω@$V_{GS}$=4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- High density cell design for low $R_{DS(ON)}$
- Voltage controlled small signal switch
- Rugged and reliable
- High saturation current capability
- The soldering temperature and time shall not exceed 260℃ for more than 10 seconds
- In compliance with EU RoHS 2011/65/EU directives
- Suffix "-H" indicates Halogen-free part, ex. 2N7002E-H

## Package outline

SOT-23




Dimensions in inches and (millimeters)

## Mechanical data

- Epoxy:UL94-V0 rated flame retardant
- Case : Molded plastic, SOT-23
- Terminals : Solder plated, solderable per MIL-STD-750, Method 2026
- Mounting Position : Any
- Weight : Approximated 0.0084 gram

## Maximum ratings (AT $T_A$=25°C unless otherwise noted)

| Parameter | Conditions | Symbol | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Drain-source voltage | | $V_{DSS}$ | | | 60 | V |
| Drain current - continuous | $T_A$=25°C | $I_D$ | | | 300 | mA |
| -pulsed(Note 1) | | | | | 1200 | |
| Gate-source voltage - continuous | | $V_{GSS}$ | | | ±20 | V |
| Gate-source voltage - non repetitive | $t_p$<50μs | | | | ±40 | |
| Power dissipation | $T_A$=25°C | $P_D$ | | | 350 | mW |
| Operating junction and storage temperature range | | $T_J$, $T_{STG}$ | -55 | | +150 | °C |
| Thermal resistance | Junction to ambient | $R_{\theta JA}$ | | | 375 | °C/W |

Note 1: Pulse width limited by safe operating area

# 2N7002E

## Electrical characteristics (AT $T_A$=25°C unless otherwise noted)

### OFF CHARACTERISTIC

| Parameter | Conditions | Symbol | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Drain-source breakdown voltage | $V_{GS}$=0V, $I_D$=250μA | $BV_{DSS}$ | 60 | | | V |
| Zero gate voltage drain current | $V_{DS}$=60V, $V_{GS}$=0V | $I_{DSS}$ | | | 1.0 | μA |
| | $V_{DS}$=60V, $V_{GS}$=0V, $T_J$=125°C | | | | 10 | μA |
| Gate-body leakage, forward | $V_{DS}$=0V, $V_{GS}$=20V | $I_{GSSF}$ | | | 100 | nA |
| Gate-body leakage, reverse | $V_{DS}$=0V, $V_{GS}$=-20V | $I_{GSSR}$ | | | -100 | nA |

### ON CHARACTERISTIC (Note1)

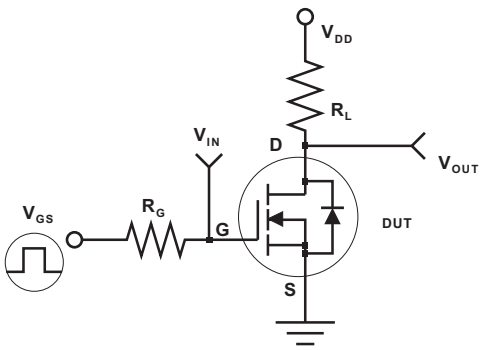
| | | | | | | |
|---|---|---|---|---|---|---|
| Gate threshold voltage | $V_{DS}$=$V_{GS}$, $I_D$=250μA | $V_{GS(th)}$ | 1.0 | 1.7 | 2.5 | V |
| Static drain-source on-resistance | $V_{GS}$=10V, $I_D$=500mA | $R_{DS(on)}$ | | 2.5 | 5.0 | Ω |
| | $V_{GS}$=4.5V, $I_D$=300mA | | | 3.3 | 5.5 | |
| Source-drain current | | $I_{SD}$ | | | 0.35 | A |
| Source-drain current (pulsed) | | $I_{SDM(2)}$ | | | 1.4 | A |
| Forward trans-conductance | $V_{DS}$=10V, $I_D$=500mA | $G_{FS(1)}$ | | 0.6 | | S |
| Diode forward Voltage | $V_{GS}$=0V, $I_S$=0.12mA | $V_{SD(1)}$ | | 0.85 | 1.5 | V |

### DYNAMIC CHARACTERISTICS

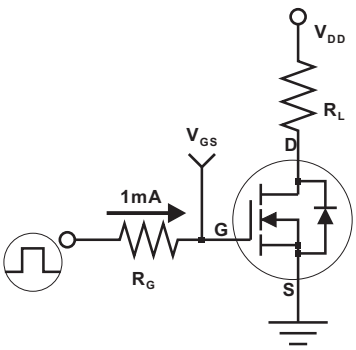
| | | | | | | |
|---|---|---|---|---|---|---|
| Input capacitance | $V_{DS}$=25V, $V_{GS}$=0V, f=1.0MHz | $C_{iss}$ | | 43 | | pF |
| Output capacitance | | $C_{oss}$ | | 20 | | |
| Reverse transfer capacitance | | $C_{rss}$ | | 6.0 | | |
| Total gate charge | $V_{DD}$=30V, $I_D$=1A , $V_{GS}$=5V | $Q_g$ | | 1.4 | 2.0 | nC |
| Gate-source charge | | $Q_{gs}$ | | 0.8 | | |
| Gate-drain charge | | $Q_{gd}$ | | 0.5 | | |
| Turn-on time | $V_{DD}$=30V, $R_G$=4.7Ω, $V_{GS}$=4.5V, $I_D$=500mA | $t_{d(on)}$ | | 6.0 | | ns |
| | | $t_r$ | | 5.0 | | |
| Turn-off time | | $t_{d(off)}$ | | 15 | | |
| | | $t_r$ | | 6.0 | | |

(1) Pulsed: Pulse duration=300μs, duty cycle1.5%.
(2) Pulse width limited by safe operating area.

**Switching Test Circuit**




**Gate Charge Test Circuit**



# Rating and characteristic curves (2N7002E)

**FIG.1 Transfer Characteristics**

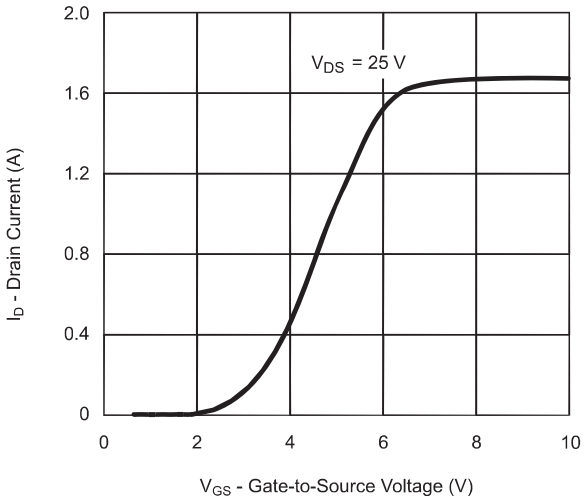



**FIG.2 On-Resistance vs. Drain Current**

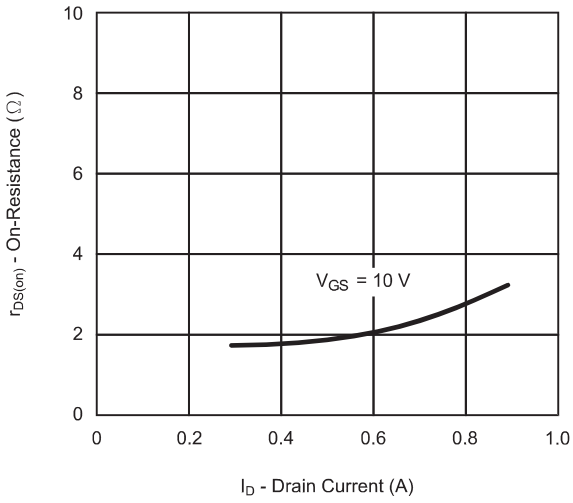



**FIG.3 Capacitance**

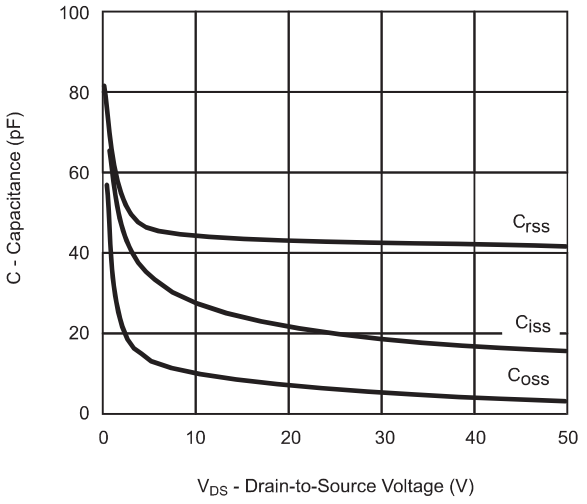



**FIG.4 On-Resistance vs. Gate-to-Source Voltag**

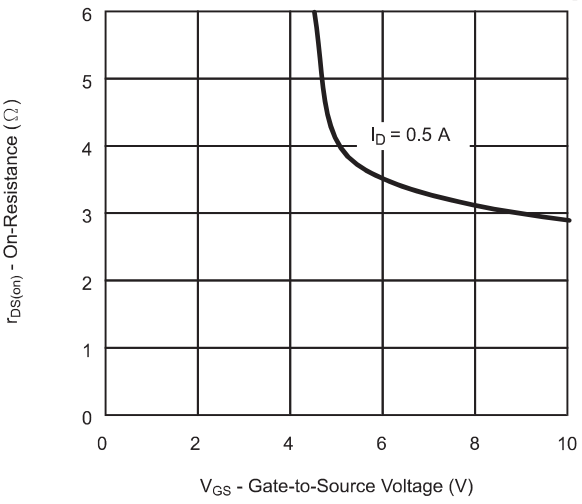



**FIG.5 Threshold Voltage**

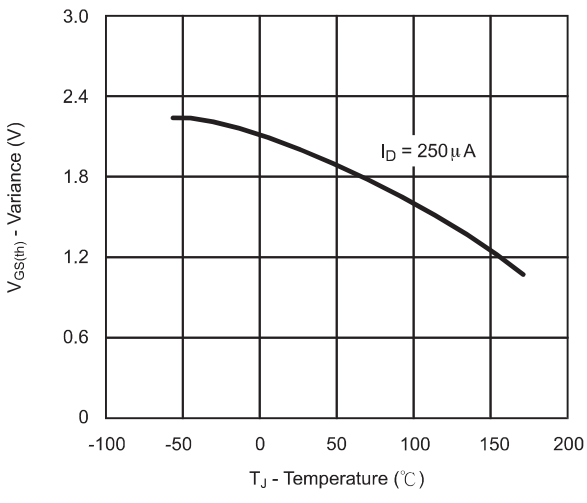
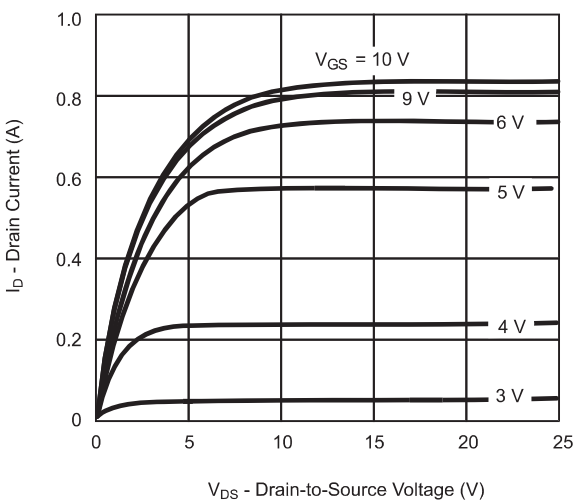



**FIG.6 On-Region Characteristics**



## Rating and characteristic curves (2N7002E)

**FIG.7** Gate Charge

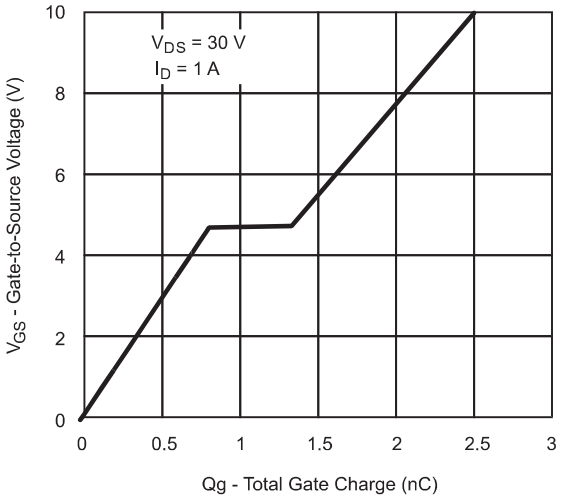



**FIG.8** On-Resistance vs. Drain Current

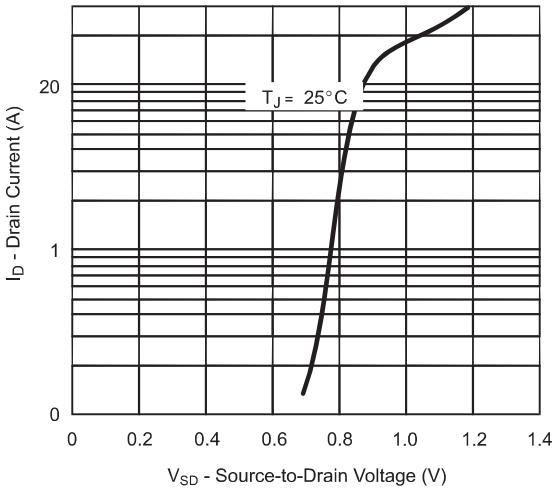



**FIG.9 Maximum Forward Biased Safe Operating Area**

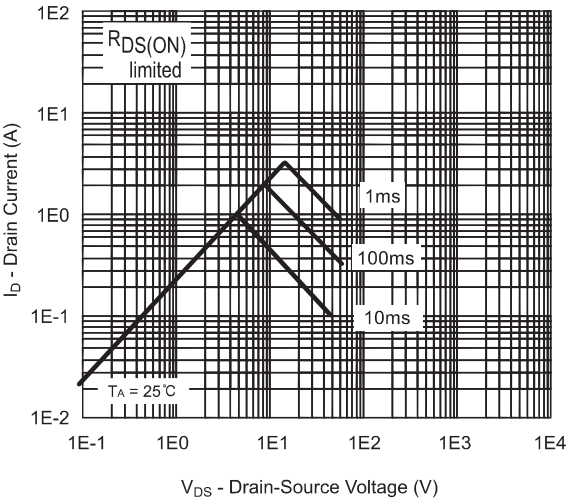
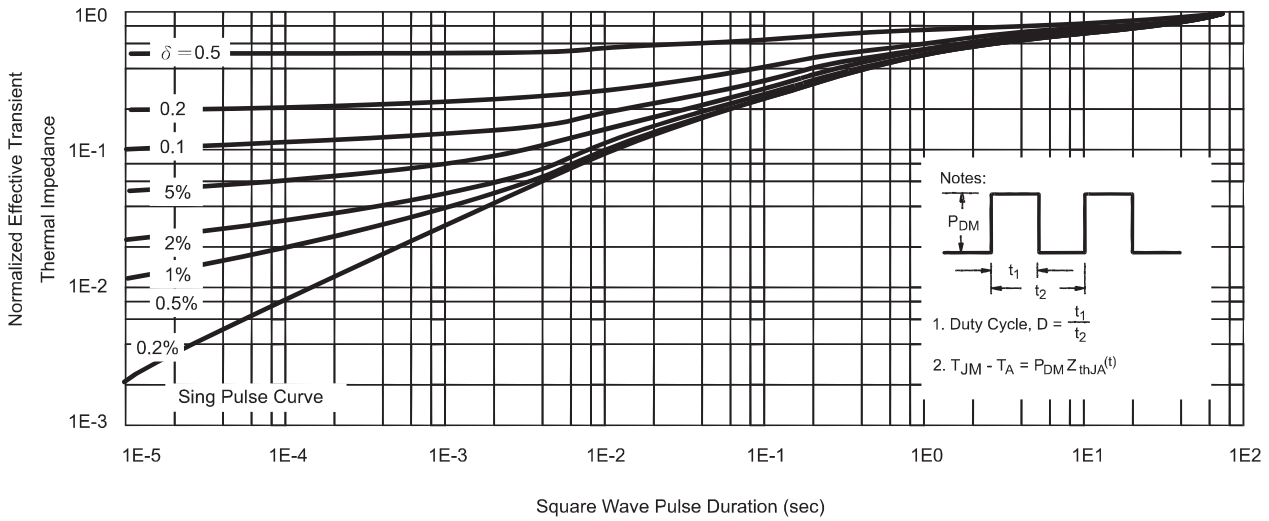
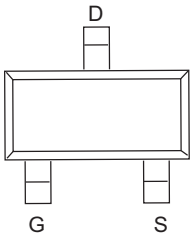
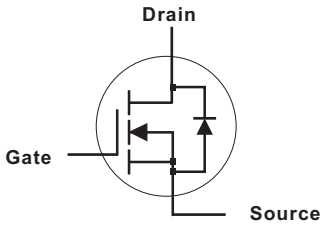



**FIG.10 Normalized Thermal Transient Impedance, Junction-to-Ambient**



# 2N7002E

## Pinning information

| Pin | Simplified outline | Symbol |
|---|---|---|
| PinD Drain<br>PinG Gate<br>PinS Source |  |  |

## Marking

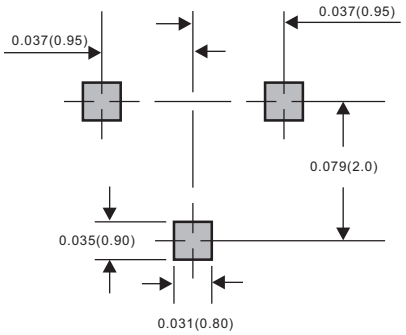
| Type number | Marking code |
|---|---|
| 2N7002E | 702≅ (Note 1) |
| | E73≅ (Note 1) |

**Note 1: ≅ = Month code**

| Month | Jan | Feb | Mar | Apr | May | Jun | Jul | Aug | Sep | Oct | Nov | Dec |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Odd Year | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | T | V | C |
| Even Year | E | F | H | J | K | L | N | P | U | X | Y | Z |

## Suggested solder pad layout

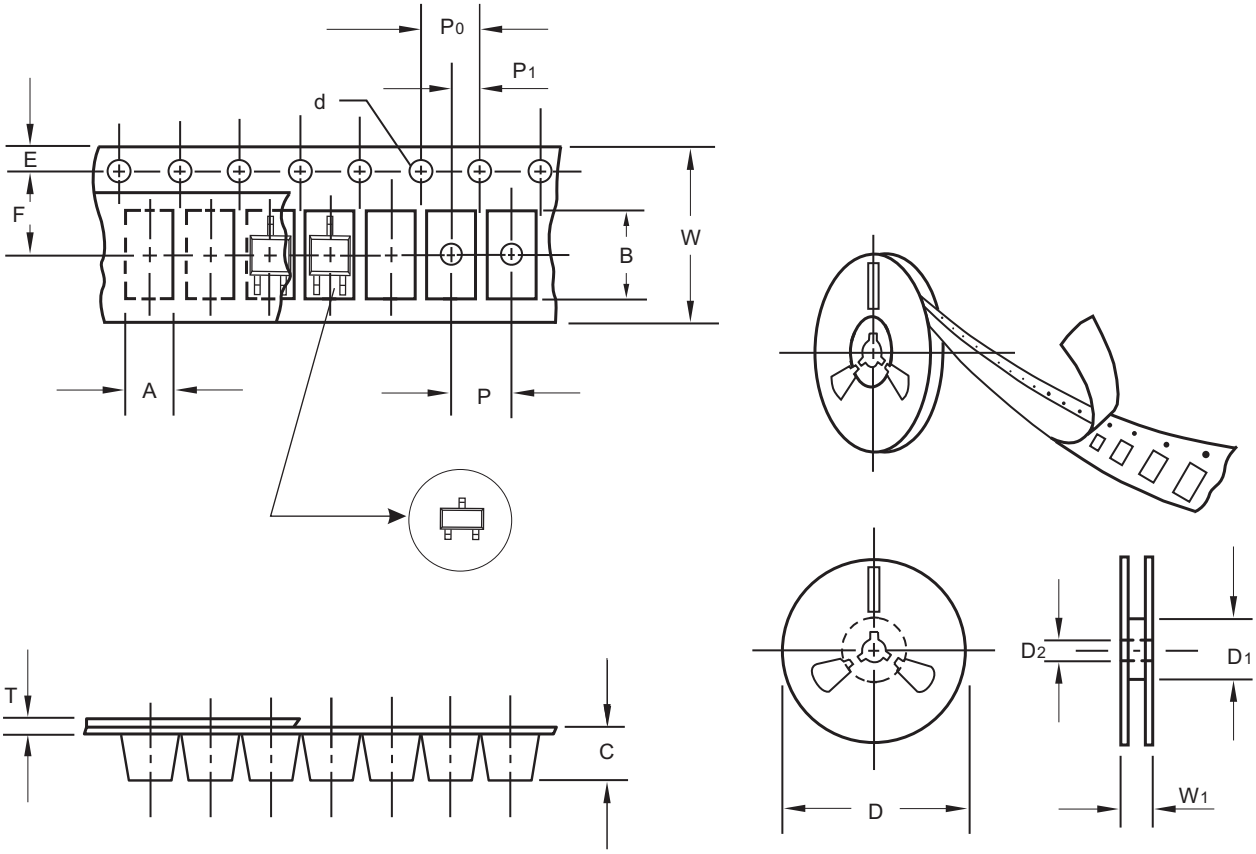
**SOT-23**




Dimensions in inches and (millimeters)

# 2N7002E

## Packing information




unit:mm

| Item | Symbol | Tolerance | SOT-23 |
|---|---|---|---|
| Carrier width | A | 0.1 | 3.15 |
| Carrier length | B | 0.1 | 2.77 |
| Carrier depth | C | 0.1 | 1.22 |
| Sprocket hole | d | 0.1 | 1.50 |
| 13" Reel outside diameter | D | 2.0 | - |
| 13" Reel inner diameter | $D_1$ | min | - |
| 7" Reel outside diameter | D | 2.0 | 178.00 |
| 7" Reel inner diameter | $D_1$ | min | 55.00 |
| Feed hole diameter | $D_2$ | 0.5 | 13.00 |
| Sprocket hole position | E | 0.1 | 1.75 |
| Punch hole position | F | 0.1 | 3.50 |
| Punch hole pitch | P | 0.1 | 4.00 |
| Sprocket hole pitch | $P_0$ | 0.1 | 4.00 |
| Embossment center | $P_1$ | 0.1 | 2.00 |
| Overall tape thickness | T | 0.1 | 0.23 |
| Tape width | W | 0.3 | 8.00 |
| Reel width | $W_1$ | 1.0 | 12.0 |

Note:Devices are packed in accor dance with EIA standar RS-481-A and specifications listed above.

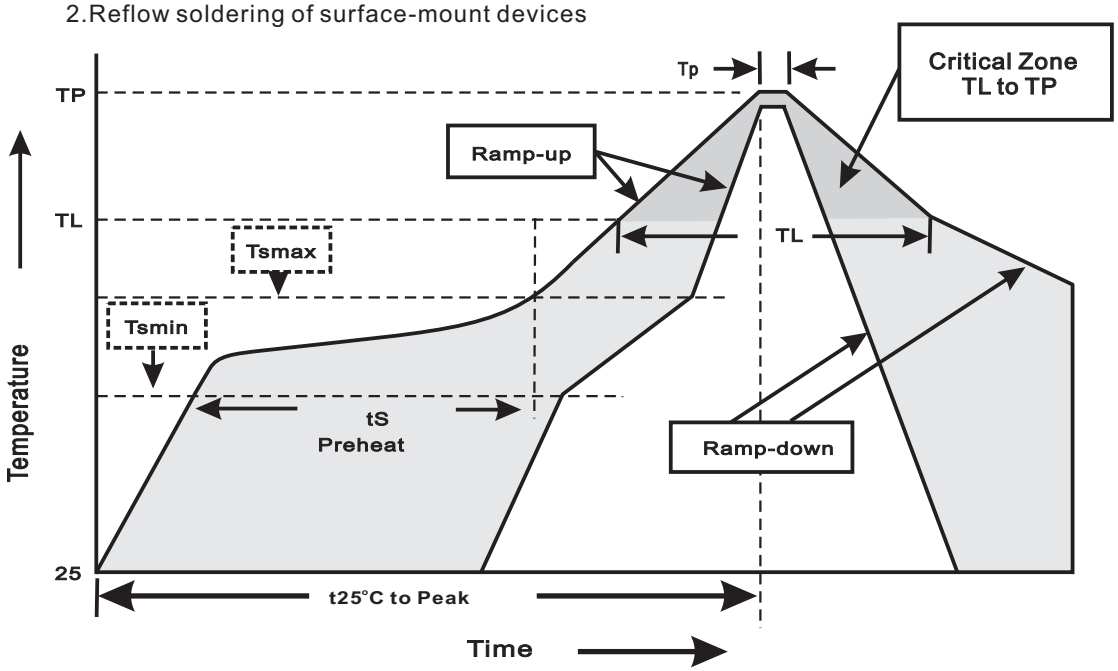
# 2N7002E

## Reel packing

| PACKAGE | REEL SIZE | REEL (pcs) | COMPONENT SPACING (m/m) | BOX (pcs) | INNER BOX (m/m) | REEL DIA, (m/m) | CARTON SIZE (m/m) | CARTON (pcs) | APPROX. GROSS WEIGHT (kg) |
|---|---|---|---|---|---|---|---|---|---|
| SOT-23 | 7" | 3,000 | 4.0 | 30,000 | 183*123*183 | 178 | 382*257*387 | 240,000 | 11.6 |

## Suggested thermal profiles for soldering processes

1.Storage environment: Temperature=5°C~40°C Humidity=55%±25%
2.Reflow soldering of surface-mount devices




3.Reflow soldering

| Profile Feature | Soldering Condition |
|---|---|
| Average ramp-up rate($T_L$ to $T_P$) | <3°C/sec |
| Preheat<br>-Temperature Min(Tsmin)<br>-Temperature Max(Tsmax)<br>-Time(min to max)($t_s$) | <br>150°C<br>200°C<br>60~120sec |
| Tsmax to $T_L$<br>-Ramp-upRate | <br><3°C/sec |
| Time maintained above:<br>-Temperature($T_L$)<br>-Time($t_L$) | <br>217°C<br>60~260sec |
| Peak Temperature($T_P$) | 255°C-0/+5°C |
| Time within 5°C of actual Peak Temperature($t_P$) | 10~30sec |
| Ramp-down Rate | <6°C/sec |
| Time 25°C to Peak Temperature | <6minutes |

# 2N7002E

## High reliability test capabilities

| Item Test | Conditions | Reference |
|---|---|---|
| 1. Solder Resistance | at 260±5°C for 10 sec. | MIL-STD-750D METHOD-2031 |
| 2. Solderability | at 245±5°C for 5 sec. | MIL-STD-202F METHOD-208 |
| 3. High Temperature Reverse Bias | $V_{DS}$=0.8 X $BV_{DSS}$, at $T_J$=150°C for 168 hrs. | MIL-STD-750D METHOD-1038 |
| 4. Pressure Cooker | 15$P_{SIG}$ at $T_A$=121°C 100%RH for 4 hrs. | JESD22-A102 |
| 5. Temperature Cycling | -55°C to +125°C dwelled for 30 min total 10 cycles. | MIL-STD-750D METHOD-1051 |
| 6. Humidity | at $T_A$=85°C, 85%RH for 1000 hrs. | MIL-STD-750D METHOD-1021 |
| 7. High Temperature Storage Life | at $T_A$=175°C for 1000 hrs. | MIL-STD-750D METHOD-1031 |